Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1-19. (Cancelled)

20. (Currently Amended) A system comprising:

a program memory;

a plurality of processors in communication with the program memory, each processor sharing the program memory among other ones of the plurality of processors;

a plurality of coprocessors separate from the plurality of processors, each coprocessor being coupled to a corresponding processor and including a field programmable gate array (FPGA); and

a shared resource manager operable to program each field programmable gate array associated with the plurality of coprocessors,

wherein a first processor of the plurality of processors is operable to execute an application and send an instruction from the program memory to each of the plurality of coprocessors to perform a function for the application,

if none of the field programmable gate ~~array~~ arrays (FPGAs) associated with the plurality of coprocessors are programmed to perform the function for the application, then the shared resource manager is operable to dynamically program any one of the field programmable gate arrays (FPGAs) to perform the function for the application, in which the field programmable gate array (FPGA) selected to be dynamically programmed is selected in accordance with a least recently used algorithm, the least recently used algorithm specifying a function that can be disabled to free up logic resources within the field programmable gate array (FPGA) selected to

be dynamically programmed.

21. (New) The system of claim 20, wherein one or more of the coprocessors further comprises an Auxiliary Processing Unit (APU) interface configured to receive instructions from the processor, the Auxiliary Processing Unit (APU) interface determining whether a given instruction is to be processed by the one or more coprocessors.

22. (New) The system of claim 21, wherein the Auxiliary Processing Unit (APU) interface is configured to issue a faulty commit if the given instruction is to be processed by the one or more coprocessors and the field programmable gate array (FPGA) in the one or more coprocessors is not programmed to perform a function corresponding to the given instruction.

23. (New) The system of claim 20, wherein the system comprises an Application Specific Integrated Circuit (ASIC) or a system-on-a-chip.